Low-order fixed denominator IIR VFD filter design

Kwan, H.K.; Jiang, A.


Abstract

A two-stage design method of low-order fixed denominator IIR variable fractional delay (VFD) digital filters is presented in this paper. In the first stage, a set of FIR fractional delay (FD) filters are designed first. Each FIR FD filter design problem is formulated in the peak-constrained weighted least-squares (PCWLS) sense and solved by the projected least-squares (PLS) algorithm. Then, model reduction technique is applied on a time-domain average FIR filter to obtain the fixed denominator. The remaining numerators of the IIR FD filters can be obtained by solving linear equations derived from the orthogonality principle. In the second stage of the design, these FD filter coefficients are to be approximated by polynomial functions of FD. Three sets of filter-examples are given to illustrate the effectiveness of the proposed design method. ©2009 IEEE.

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Authors’ affiliation
KHK; JA: Department of Electrical and Computer Engineering, University of Windsor, 401
Sunset Avenue, Windsor, ON N9B 3P4, Canada
Correspondence address
Kwan, H. K.; Department of Electrical and Computer Engineering, University of Windsor, 401 Sunset Avenue, Windsor, ON N9B 3P4, Canada; email: kwan1@uwindsor.ca